

Consumer Video Kit (CVK) Getting Startup Guide

Rev. 1.00

Revision History

Rev	Date	Description	By
0.01	2010/3/1	Preliminary release	Nagatani
0.02	2010/4/28	Initial release	Nagatani
1.00	2010/05/11	Release Version	Nagatani

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1. Overview

This documentation describes an overview of reference designs attached on Consumer Video Kit Pro Kit (CVK-PRO).

2. Table of reference designs

The following are overview of each reference design.

LVDS Reference Design

7:1 LVDS Loop-back Test Design

HDMI Reference Design

HDMI Input and Output Design and one Frame Buffer function

V-by-One® HS Reference Design

HDMI Input to V-One HS Output Design (Included Time Bom IP)

V-by-One HS Input to HDMI Output Design (Included Time Bom IP)

Display-Port Reference Design

A bitstream data for CVK-PRO will be provided from Xilinx web site.

(URL: <http://www.xilinx.com/products/ipcenter/EF-DI-DISPLAYPORT.htm>)

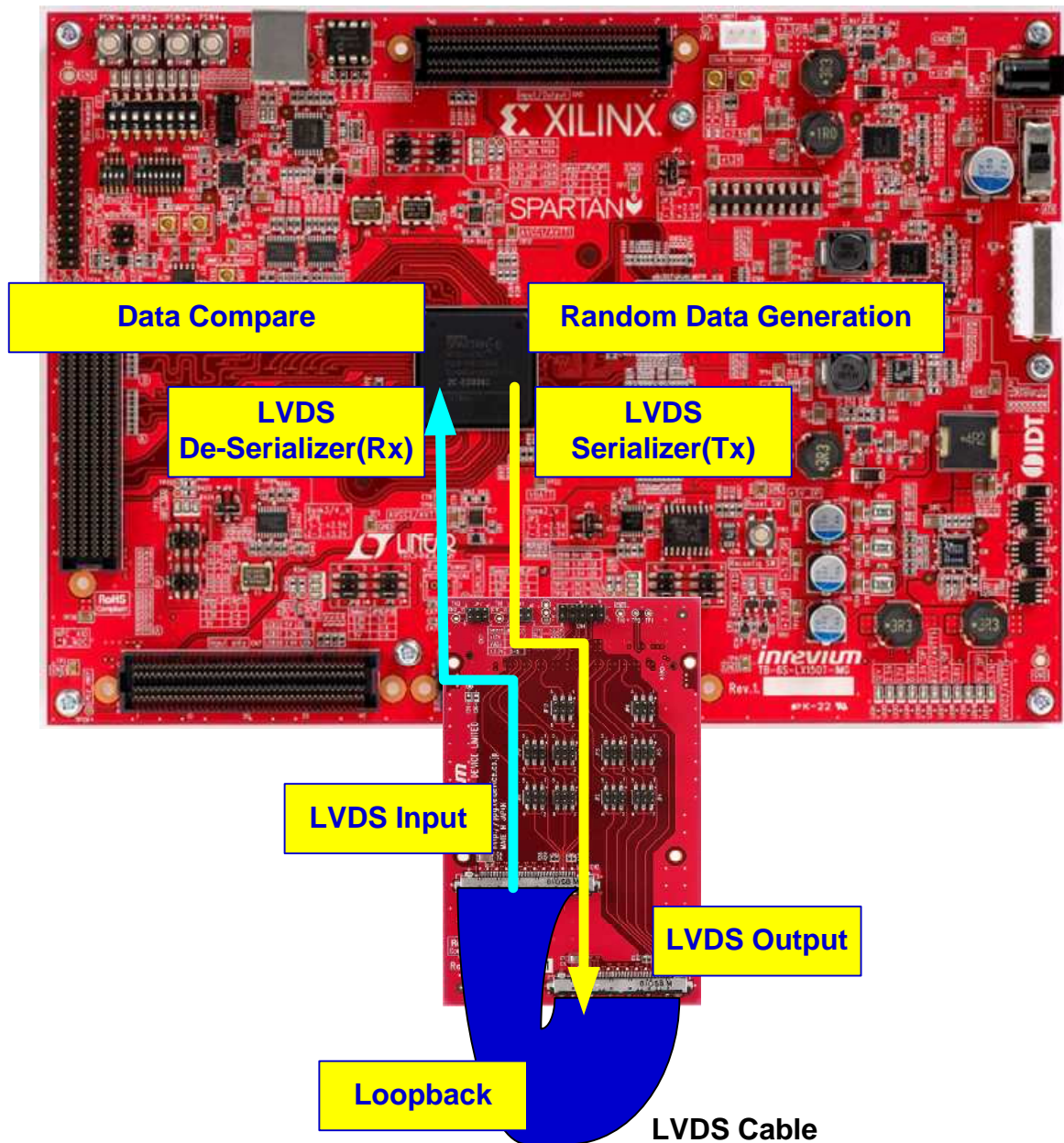
3. LVDS Reference Design

- Design Overview.

Data pass: Pattern Data Output > TB-FMCL-LVDS > Loop Back (Cable) >

TB-FMCL-LVDS > Data Compare

Data rate: 519.75Mbps, 7:1 serialize LVDS interface



4. HDMI Reference Design

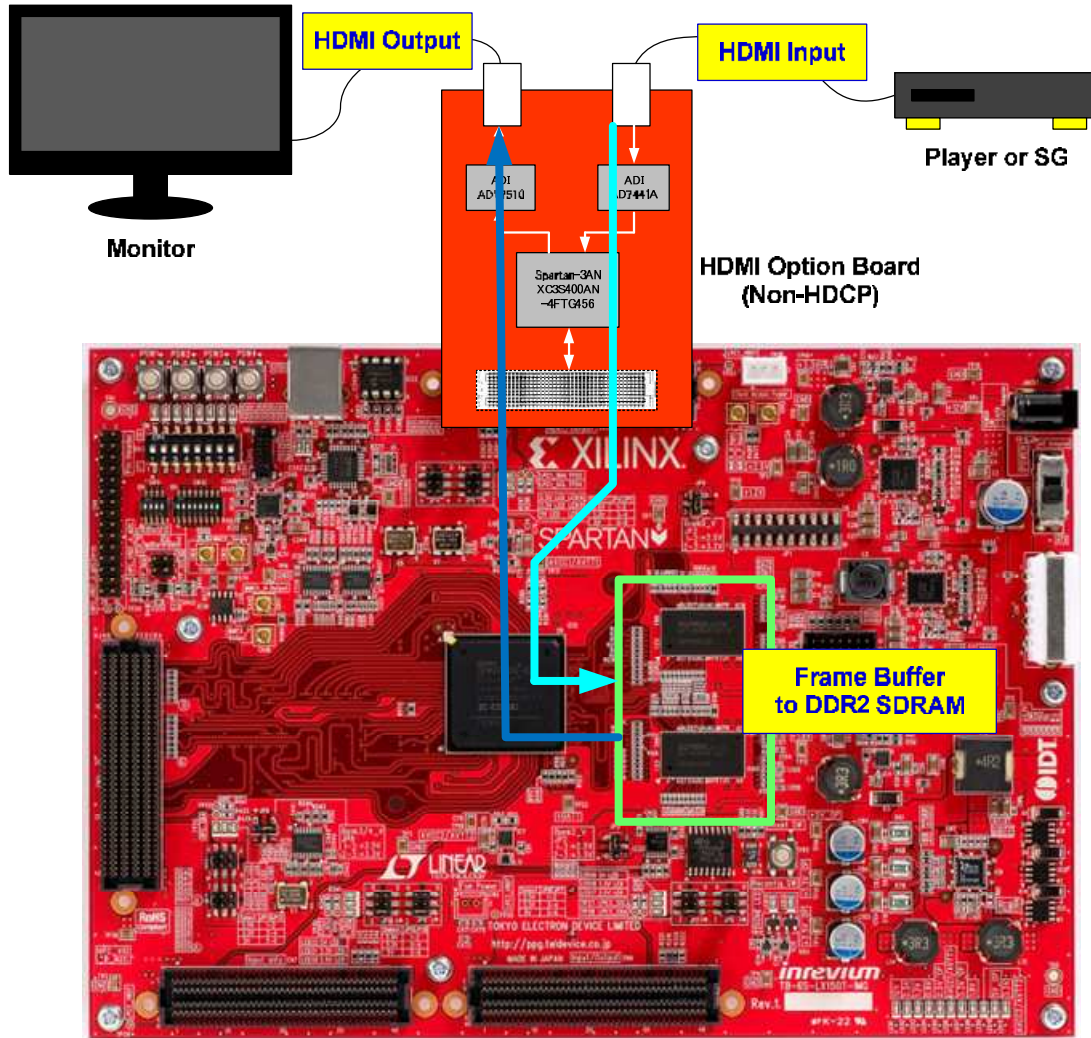
- Design Overview.

Data Pass: TB-FMCL-HDMI input > DDR2SDRAM > TB-FMCL-HDMI output

Picture resolution: 1080/60p

Frame Buffer: Integrated Memory controller, DDR2SDRAM, One frame buffering

Notice: TB-FMCL-HDMI does not support HDCP. Please check player equipment.



5. V-by-One® HS Reference Design

■ Design Overview1

Data Pass: TB-FMCH-Vby1 input > TB-6S-150T-IMG > TB-FMCL-HDMI output.

Data rate: 2.97Gbps (V-by-One HS)

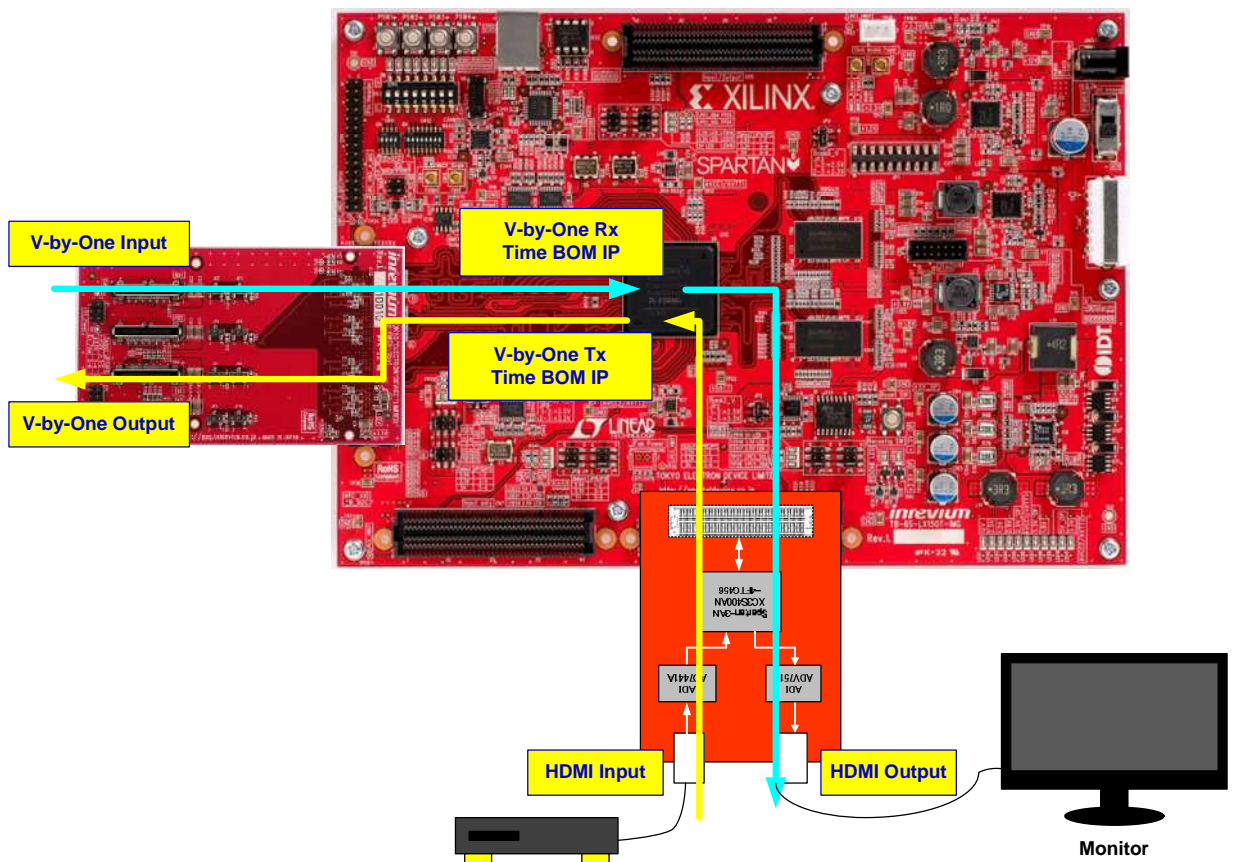
Picture resolution: 1080/60p (HDMI)

■ Design Overview2

Data Pass: TB-FMCL-HDMI input > TB-6S-150T-IMG > TB-FMCH-Vby1 output.

Data rate: 2.97Gbps (V-by-One HS)

Picture resolution: 1080/60p (HDMI)



■ Functional Limitation

This sample design assumes the following operational characteristics:

- Video resolution

up to 10bit color RGB Full-HD (1080p/60Hz @ 148.5MHz pixel clock) image

- Number of Data Lanes

2 data lanes (Data rate per lane is 2.97Gbps)

- Maximum time for continuous operation

Approx. 2 hours (FPGA needs to be reconfigured for return operation)

6. Display-Port Reference Design

The DisplayPort IP core available in IDS version 11.4 via CoreGen will be enhanced in IDS 12.1 to fully support the DisplayPort FMC included in the CVK-PRO.

A link to a bitstream for a system level design and Xilinx XCELL article titled *An FPGA Route Toward Implementing DisplayPort* can be found in the Documentation section (see example below) of the Xilinx DisplayPort Center IP web page available with **IDS 12.1**.

The screenshot shows the Xilinx website for the LogiCORE DisplayPort product. The page is titled "LogiCORE DisplayPort" and features a navigation menu with options like "Product & Services", "Technology Solutions", "Market Solutions", "Support", "Buy Online", and "About Xilinx". The main content area is divided into sections: "Product Information" and "Resources". The "Resources" section is highlighted, showing a list of documents: "DisplayPort", "Release Notes (PDF)", and "Core Site License Agreement (PDF)", which are circled in red. Other sections include "Need Help?", "Product Details", "Documentation", and "Device Family Support".

URL: <http://www.xilinx.com/products/ipcenter/EF-DI-DISPLAYPORT.htm>

A system level reference design with source code, implementation scripts and documentation *XAPP: Implementing a DisplayPort Source Policy Maker using a MicroBlaze embedded system* will be available end of May.



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